WHAT IS CLAIMED IS:

1. An electrical router backplane comprising:

a first plurality of card slots, each capable of mating with the backplane electrical connector sets of a packet input/output card to couple electrical signals from that packet input/output card to a corresponding set of signaling thru-holes in the backplane;

a second plurality of card slots comprising at least three card slots, each capable of mating with the backplane electrical connector sets of a switch fabric card to couple electrical signals from that switch fabric card to a corresponding set of signaling thru-holes in the backplane; and

multiple embedded high-speed signaling layers, each sandwiched between corresponding upper and lower dielectric material layers separating that signaling layer respectively from upper and lower ground planes, each high-speed signaling layer comprising differential trace pairs, each trace pair forming point-to-point connections between two pairs of the signaling thru-holes, such that, collectively, the high-speed signaling layers contain at least two differential trace pairs to connect each first card slot with each second card slot.

2. The backplane of claim 1, each differential trace pair configured with an individual trace width of approximately 7 to 9 mils and a trace height, differential trace spacing, and trace-to-ground-plane spacing related to trace width such that the impedance of a given trace is marginally more differential than single-ended.

3. The router backplane of claim 2, wherein the individual trace width is approximately 8 mils, the differential trace height is approximately 1.4 mils, the differential trace

spacing is approximately 16 mils, and the trace-to-ground-plane spacing is approximately 6 to 8 mils.

4. The router backplane of claim 2, wherein the individual trace width is approximately 7 mils, the differential trace height is approximately 1.4 mils, the differential trace spacing is approximately 17 mils, and the trace-to-ground-plane spacing is approximately 6 to 8 mils.

5. The router backplane of claim 2, wherein the differential and single-ended impedance values of a given trace are approximately equal to the intrinsic impedance of the dielectric material.

6. The router backplane of claim 5, wherein the differential impedance is slightly less than the intrinsic impedance and the single-ended impedance is slightly greater than the intrinsic impedance.

7. The router backplane of claim 2, each card slot having a connector region comprising rows of signaling thru-holes alternating with rows of ground thru-holes, the ground thru-holes connected to the ground planes, wherein each high-speed signaling layer has a plurality of differential trace pairs routed through one or more connector regions such that, for any given one of those trace pairs, that trace pair passes through a connector region in an alignment that intersects a row of ground thru-holes, such that where that trace pair approaches a ground thru-hole, the traces of that differential trace pair separate as they approach that ground thru-hole, pass on opposite sides of that thru-hole, and rejoin into a differential configuration on the opposite side of that

thru-hole.

8. The router backplane of claim 7, wherein as the traces of a differential pair pass on opposite sides of a ground thru-hole, each of those two traces maintains a separation from that thru-hole approximately equal to the trace-to-ground-plane spacing for that differential pair.

9. The router backplane of claim 7, wherein the alignment of a given one of those differential trace pairs routed through a connector region is centered with respect to the thru-hole, and wherein the two traces of that pair separate, as they approach the thru-hole, at approximately a 90-degree angle until the two traces are separated by more than the clearance required for the thru-hole, pass the thru-hole parallel to each other, and then rejoin at approximately a 90-degree angle until reaching the differential configuration.

10. The router backplane of claim 1, wherein the initial segments of two traces of a differential pair are length-matched by the inclusion of a looped jog near the signal-insertion end of the nominally shorter of the two trace segments.

11. The router backplane of claim 10, wherein the jog further compensates for path length differences in a card backplane electrical connector, between the connector signal paths corresponding to the first and second traces.

12. The router backplane of claim 1, wherein the first and second pluralities of card slots are arranged respectively in first and second ranks, the first and second ranks spaced

apart to form a differential trace routing area between the ranks.

13. The router backplane of claim 12, wherein, for the majority of the high-speed signaling layers, each layer contains substantially all of the differential trace pairs connecting each first card slot to a selected one of the second card slots.

14. The router backplane of claim 12, further comprising power distribution planes embedded between adjacent ground plane layers, each card slot coupled to the power distribution planes at power thru-holes corresponding to power connectors on the cards, the power thru-holes located outboard of the signaling thru-holes for each card slot.

15. The router backplane of claim 12, further comprising a card slot for a route processing module, that card slot having substantially more signaling thru-holes than either a packet input/output card slot or a switch fabric card slot, the route processing module card slot located within the first rank of card slots, substantially in the middle of that rank.

16. The router backplane of claim 1, wherein the longest differential pairs are routed on the bottommost high-speed signaling layers, with the backplane bottom high-speed signaling layer defined as the layer furthest from the card slot side of the thru-holes connected to those differential pairs.

17. The router backplane of claim 1, wherein the high-speed signaling layers are arranged within the backplane according to the longest differential pairs on each signaling

layer, such that the topmost signaling layers have shorter longest differential pairs than the bottommost signaling layers, with the backplane bottom high-speed signaling layer defined as the layer furthest from the card slot side of the thru-holes connected to the differential pairs.

18. The router backplane of claim 1, further comprising low-speed signaling traces, the correspondence of signaling thru-holes to traces arranged, for the majority of the high-speed differential pairs, such that high-speed differential pairs connect to signaling thru-holes adjacent to signaling thru-holes that are either connected to low-speed signaling traces or unconnected.

19. The router backplane of claim 18, wherein the signaling thru-holes are arranged in rows of six holes, such that for the majority of the rows of signaling thru-holes, the outermost two holes on each end of a row connect to the traces of a high-speed differential pair, and the innermost two thru-holes do not.

20. The router backplane of claim 18, wherein the majority of the low-speed signaling traces reside on low-speed signaling layers separate from the high-speed signaling layers.